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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,700	09/14/2005	Wade A. Krull	211843-00030	6925

27160 7590 01/08/2007

PATENT ADMINISTRATOR
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EXAMINER	
ANGADI, MAKI A	
ART UNIT	**PAPER NUMBER**
1765	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/519,700	KRULL, WADE A.	
	Examiner	Art Unit	
	Maki A. Angadi	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/23/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-7, 9, 12, 15 and 20-23 are rejected under 35 U.S.C. 103(a) over Lin (US Patent No. 6,069,061) in view of Taniguchi (US Patent No. 6,690,050).

As to claim 1, 11 17 and 19, Lin discloses a method for forming a gate electrode for a metal oxide semiconductor device (col.1, lines 11-16) having a substrate (300) (Fig.1A) and formed with a well and opposing trench isolation portions (102) with a first dielectric layer (302) formed thereon (Fig.3A) (col.3, lines 36-37), the method includes the steps of: (a) depositing a first gate electrode layer (304) on first dielectric layer (col.3, lines 39-40); (b) doping first gate electrode layer (304), defining a doped first gate electrode layer (col.3, lines 42-44); (c) depositing a second gate electrode layer (306) on the doped first gate electrode (col.3, lines 46-47); (c) depositing a second gate electrode layer(308) on doped first gate electrode layer (col.3, lines 47-48); (d) doping second gate electrode layer (col.3, lines 50-52); (e) forming a gate stack from the combination of doped first gate electrode layer and said second gate electrode, resulting exposed portions of the first dielectric layer (Fig.3C, col.3, lines 55-60); (f)

patterning a second photoresist layer to form spacers (411) (Fig.4C) to define drain/source (412) regions (col.5, lines 4-9); (g) depositing a second gate dielectric layer different than first dielectric layer on exposed surface of first dielectric layer (Fig.3A and 3B) (col.3,lines 36-37 and lines 46-47).

Lin discloses photolithography and etching to form gate structure (col.3, lines 55-56) but is silent about patterning a first and second photoresist to expose drain extensions. However, Taniguchi discloses patterning a first photoresist layer (14) and removing it (col.7, line 1) to form CMOS gate electrode (13b) (Fig. 2A) (col.7, lines 5-7) on dielectric layer adjacent to trench isolation portions (12) and defining source and drain regions (16) (Fig.2B) (col.7, lines 16-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select patterning photoresist in the formation of source and drain regions because Taniguchi illustrates that patterning and etching of the photoresist facilitates the formation of source and drain regions on either side of trench isolation structures.

Lin fails to disclose the process of heat-treating the structure to activate the dopant material. However, Taniguchi discloses heat treatment for about 10 second at 1000°C by rapid thermal annealing (col.8, lines 23-26). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select heat treatment of the structure fabricated by Lin because Taniguchi illustrates that heat treatment is employed to activate the implanted ions (col.8, line 26).

Lin fails to disclose forming second gate electrode stack to be offset and larger than gate stack formed from first gate electrode layer. However, Taniguchi discloses the second gate electrode stack to be offset and larger that the first gate stack layer (Fig.5B) (col.8, lines 53-64). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select spacing of first and second gate electrode layer because Taniguchi illustrates that the spacing of first and second gate electrode improves transistor characteristics the manufacture yield (col.5, lines 60-62).

As to claim 2, Lin discloses the first gate electrode layer and second gate electrode layer together for a full thickness gate electrode (Fig.3C) (col.3, lines 55-58).

As to claims 3 and 5, Lin discloses the step of depositing a first and second gate electrode layer that includes depositing amorphous silicon (col.4, lines 5-8).

As to claims 4 and 6, Lin discloses the step of depositing a first and second gate electrode layer includes depositing polysilicon (col.3, lines 55-58).

As to claims 7, 9 and 12, Lin discloses the step of doping first and second gate electrode layer includes doping with boron (col.3, lines 42-44, col.3, lines 51-53).

As to claim 15, Lin discloses implanting arsenic ions into the source/drain regions (col.6, lines 4-6) but is silent about boron. However, Taniguchi discloses implanting boron into the source and drain regions (col.7, lines 18-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to dope boron into the source/drain regions described by Lin because Taniguchi illustrates that boron doping will not enter the gate insulating film so that the transistor characteristics can be maintained stable during operation (col.4, lines 56-60).

As to claim 20-23 Lin discloses the implanting gate structure (Fig.3D) (col.4, line 1-8) but fails to disclose chemical treatment, removal of first dielectric layer, implanting of species into the first gate oxide layer and thickness of first and second gate electrode. However, Taniguchi discloses the process of thermal oxidation, which introduces oxygen into the oxide layer (col.6, lines 56-59) and chemical treatment of the structure (col.6, lines 60-67) and removal of oxide layer (col.8, lines 27-30) and re-growth of second dielectric material different from the first dielectric material (col.7, lines 39-42)(Fig.3B) and thickness of first and second gate electrode in the range of about 250 nm (col.8, lines 52-64), which is approximately the thickness of the conventional gate electrode. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select chemical treatment, removal of dielectric layer in the process employed by Lin because Taniguchi illustrates that the steps in the

formation of gate electrode structure would maintain stable transistor characteristics (col.4, lines 59-60).

Claim Rejections - 35 USC § 103

2. Claims 8, 10 and 18, are rejected under 35 U.S.C. 103(a) over Lin (US Patent No. 6,069,061) in view of Taniguchi (US Patent No. 6,690,050) as applied to claim 1 above, in further view of Goto (US Patent No. 6,013,332).

Lin fails to disclose doping of gate electrode and doping drain extension regions with decaborane. However, Goto discloses the process of doping decaborane into the gate electrode and drain extensions (Fig.11) (col.7, lines 42-46, lines 53-55). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select decaborane for doping into the gate structures of Lin because Goto illustrates that mass of decaborane is ten times as large as that of boron and the effective dose will become 10 times smaller compared to boron (col.2, lines 55-58) thereby suppressing the charging phenomen (col.3, lines 1-4).

Claim Rejections - 35 USC § 103

3. Claims 13 and 16 are rejected under 35 U.S.C. 103(a) over Lin (US Patent No. 6,069,061) in view of Taniguchi (US Patent No. 6,690,050) as applied to claim 11 above, in further view of Mannino, *Nuclear Instruments and Methods in Physics Research B186, (2002) pages 246-255.*

Lin fails to disclose doping of boron clusters in the source/drain regions. However, Mannino discloses the advantage of doping boron clusters by ion implantation in the formation of shallow junctions (page 247, col.1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select boron clusters for doping source/drain regions because Mannino illustrates that doping of boron clusters lead to the realization of ultra-shallow p+ source/drain structures within 100 nm from the surface (page 247).

Claim Rejections - 35 USC § 103

4. Claim 14 is rejected under 35 U.S.C. 103(a) over Lin (US Patent No. 6,069,061) in view of Taniguchi (US Patent No. 6,690,050) as applied to claim 11 above, in further view of Gardner (US Patent no. 5,885,877).

Lin fails to disclose molecular implant into the gate electrode layer. However, Gardner discloses nitrogen molecule implant into the gate electrode (col.4, lines 53-60). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select molecular implant in the structure disclosed by Lin because Gardner illustrates that by doping molecular nitrogen into the gate electrode one can provide diffusion-retarding barrier layer against dopant diffusion into the gate dielectric layer (col.2, lines 47-52).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 24, 25, 26 and 29 are rejected under 35 U.S.C. 102(b) over Lee (US Patent No. 5,773,337).

As to claim 24 and 29, Lee discloses a process of forming an ultra-shallow junction in a semiconductor (that includes silicon) substrate that includes steps of: (a) depositing a dielectric layer (5) on a substrate (1) (Fig.2A) (col.2, lines 43-47); (b) doping said dielectric layer (col.2, lines 48-65); (c) providing heat treatment to cause implanted ions to diffuse into substrate for a shallow junction (col.3, lines 5-18, lines 38-44).

As to claims 25 and 26, Lee discloses that the doping of dielectric layer is with a single ion implant (col.2, line 59) and series of ion implants (col.2, lines 62-65).

Claim Rejections - 35 USC § 103

6. Claim 27 are rejected under 35 U.S.C. 103(a) over Lee (US Patent No. 5,773,337) as applied to claim 24 above, in view of Mannino, *Nuclear Instruments and Methods in Physics Research B186, (2002) pages 246-255.*

Lee fails to disclose doping of boron clusters in the source/drain regions. However, Mannino discloses the advantage of doping boron clusters by ion implantation in the formation of shallow junctions (page 247, col.1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select boron clusters for doping source/drain regions because Mannino illustrates that doping of boron clusters lead to the realization of ultra-shallow p+ source/drain structures within 100 nm from the surface (page 247).

Claim Rejections - 35 USC § 103

7. Claim 28 are rejected under 35 U.S.C. 103(a) over Lee (US Patent No. 5,773,337) as applied to claim 24 above, in view of Marinskiy, Materials Research Society Symposium Proceedings, Vol.669, (2001), page J2.5.1-J2.5.6.

Lee discloses doping boron into the dielectric layer but fails to disclose doping boron implant followed by hydrogen. However, Marinskiy studies the passivation of boron by hydrogen in silicon IC fabrication (page J2.5.1). Therefore, it would have been obvuious to one of ordinary skill in the art at the

time the invention was made to modify boron doping with hydrogen because Marinskiy illustrates the passivation of boron by hydrogen introduced into Si during typical surface treatment used in IC fabrication.

Claim Rejections - 35 USC § 103

8. Claim 30 are rejected under 35 U.S.C. 103(a) over Lee (US Patent No. 5,773,337) as applied to claim 24 above, in view of Muller (US Patent No. 6,693,051).

Lee discloses the use of gate oxide for a gate electrode (col.2, lines 46-47) but fails to disclose using silicon dioxide. However, Muller discloses the use of silicon oxide and silicon oxide as gate dielectric layer (60) in the gate electrode (70) (Fig.2) (col.4, lines 15-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select SiO and/or SiO2 as gate dielectric layer in the gate structure used by Lee because Muller illustrates that SiO and SiO2 increase the input capacitance per unit area of the device (col.4, lines 15-16).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Aronowitz (US Patent No. 5,837,598) discloses diffusion barrier for polysilicon gate electrode of MOS device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maki A. Angadi whose telephone number is 571-272-8213. The examiner can normally be reached on 8 AM to 4.30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dr. Maki Angadi
Examiner
Art Unit 1765

SHAMIM AHMED
PRIMARY EXAMINER